Notice of Allowability	Application No. 10/092,306	Applicant(s) FUJIYAMA, HIROYUKI	
	Examiner Bao Q Truong	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 30 August 2004*.
2. ☒ The allowed claim(s) is/are *1-2, 5-6, 8-9, and 11-12 now renumbered as 1-8 respectively*.
3. ☒ The drawings filed on *07 March 2002* are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. ______ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20040920* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Response to Amendment

1. The examiner acknowledges the applicant's submission of Amendment for Application No. 10/092,306 dated on 30 August 2004. At this point, claims 3-4, 7, and 10 have been cancelled; claims 1, 5, 8, and 11-12 have been amended. There are 8 claims pending in the application; there are 5 independent claims and 3 dependent claims, all of which are ready for reconsideration by the examiner.

Examiner's Amendment

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney J. Randall Beckers (Reg. No. 30,358) on 20 September 2004 at 11:20 am ET.

The application has been amended as follows:

Claim 11. (Currently Amended) A method for controlling a semaphore in a system including at least one processor <u>*and a bus-arbitration control circuit*</u>*, comprising:*

asserting a control signal when the processor performs a read access to a semaphore address;

<u>*said bus-arbitration control circuit*</u> *receiving a signal indicative of a bus-arbitration request, the control signal, and a chip enable signal output from the processor;*

negating the control signal when the processor performs a write access to the semaphore address, and a right to use a bus give to the processor is not relinquished in response to the bus arbitration request supplied from an external source during an asserted state of the control signal; and

said bus-arbitration control circuit operating not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal when the control signal is in the asserted state, operating not to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in an asserted state and the control signal is in a negated state, and operating to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in a negated state and the control signal is in the negated state.

Allowable Subject Matter

3. Claims 1-2, 5-5, 8-9, and 11-12 are allowed.

4. The following is an examiner's statement of reasons for allowance:

Claim 1 is allowable for the combination including the limitation of

"a bus-arbitration control circuit which receives a signal indicative of a bus-arbitration request, the control signal, and a chip enable signal output from the processor; and

said bus-arbitration control circuit operating not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal when the control signal is in the asserted state, operating not to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in an asserted state and the control signal is in a negated state, and operating to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in a negated state and the control signal is in the negated state."

Claim 5 is allowable for the combination including the limitation of

"a bus-arbitration control circuit which receives a signal indicative of a bus-arbitration request, the control signal, and a chip enable signal output from the processor; and

said bus-arbitration control circuit operating not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal when the control signal is in the asserted state, operating not to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in an asserted state and the control signal is in a negated state, and operating to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in a negated state and the control signal is in the negated state."

Claim 8 is allowable for the combination including the limitation of

"a bus-arbitration control circuit which receives a signal indicative of a bus-arbitration request, the control signal, and a chip enable signal output from the processor

said bus-arbitration control circuit operating not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal when the control signal is in the asserted state, operating not to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in an asserted state and the control signal is in a negated state, and operating to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in a negated state and the control signal is in the negated state."

Claim 11 is allowable for the combination including the limitation of

"receiving a signal indicative of a bus-arbitration request, the control signal, and a chip enable signal output from the processor; and

said bus-arbitration control circuit operating not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal when the control signal is in the asserted state, operating not to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in an asserted state and the control signal is in a negated state, and operating to assert the bus-arbitration-acknowledge signal in response to

the bus-arbitration request signal when the chip enable signal is in a negated state and the control signal is in the negated state."

Claim 12 is allowable for the combination including the limitation of

"a bus-arbitration control circuit which receives a signal indicative of a bus-arbitration request, the control signal, and a chip enable signal output from the processor; and

where said bus-arbitration control circuit operating not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal when the control signal is in the asserted state, operating not to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in an asserted state and the control signal is in a negated state, and operating to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in a negated state and the control signal is in the negated state."

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (703) 308-7090. The examiner can normally be reached on Monday-Friday from 6:00 AM to 3:00 PM (ET).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

BAO QUOC TRUONG

BT

Patent Examiner

20 September 2004

Donald Sparks

Supervisory Patent Examiner

Technology Center 2100